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A High Efficiency DC/DC Converter for High Voltage Gain High Current Applications

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Abstract— A new class of high-voltage-gain DC-DC converters for high efficiency and transformer-less DC-DC applications where large voltage step-up ratios are required, is presented in this paper. The converter is derived from the hybrid integration of a switched-capacitor converter and a boost converter. It features high step-up voltage conversion ratio with a moderate duty cycle; non-pulsating input current; low voltage stress on all of the switches; easy implementation of control and driving circuits; scalability for high current high-power applications; and low cost due to reduced components via combination of a two-stage converter into a single-stage converter. Full soft-charging operation and minimal device voltage stresses are achieved under all operating conditions. Steady-state operations of the converter are comprehensively analyzed. A 300 W prototype of a 19-time converter achieving the peak efficiency of 96.1% is built. Both simulation and experimental results validating the theoretical analysis and operation of the converter are provided.

***Index Terms*—High frequency hybrid converter, high voltage conversion ratio, low cost, high efficiency, low voltage stress, DC microgrids.**

I. INTRODUCTION

With high penetrations of distributed generations (DGs) based on renewable energy sources (RES), the traditional power grid architecture, consisting of large power generation plants, transmission and distribution networks, shall be replaced by several microgrids in an inter-grid scenario [1]. For example, DC microgrids are applicable in commercial building applications, data centers, automotive, aerospace and shipboard systems [1-7]. These applications coordinate motor drives, lighting systems, and energy storage systems using a DC bus for power distribution. To make sure these DC voltage buses feeding low voltage loads like data centers with high power quality and energy efficiency, a high-gain high-efficiency DC/DC converter is required.

DC/DC buck converter, gaining the merits of low number of active switches and passive components, is conventionally adopted to perform the step-down conversion. However, the efficiency of the DC/DC buck converter drops significantly for extremely large duty cycle. Normally, the voltage gain of conventional buck DC/DC converter is limited due to the large power losses at high voltage gain [4-5]. Therefore, they are not suitable for high-voltage-gain applications. A two-stage converter comprising two buck converters that are connected in cascade has been proposed to achieve a high voltage gain [8]. However, a set of synchronized controllers would be required to control the respective active switching devices of the two stages of the converter, so that the beat-frequency phenomenon may be avoided. This causes complexity in the design of the controller [8]. In addition, instability can easily occur when input voltage and load conditions varied [9].

One promising non-isolated DC/DC converter that can provide a high voltage gain with a high efficiency is switched-capacitor (SC) based converter [10-18]. It is easy for SC converter to achieve small size and high-power density because of the absence of magnetic components [19-29]. Several popular high-voltage-gain SC converters (series-parallel converters, Fibonacci (FIB) SC converters, and Dickson SC converters, etc.) are reported in previous literatures [30-36]. Normally, the SC converter cannot simultaneously achieve good line and load regulation, and high efficiency [37-40]. If an accurate regulation is desired, the efficiency will be severely sacrificed [42-44]. Two-stage DC/DC conversion can be adopted to solve the regulation issue and also further increase voltage gain. Because of regulation issue and achieving high voltage gain without large number of components, conventional buck converter is adopted as second stage due to its low component count and simple operation. Besides, buck converter with multi-phase operation can have high current capability in high power applications. Therefore, one common solution to solve the regulation issue and also further increase voltage gain is to use two-stage DC/DC conversion, which consists of a high voltage gain SC converter stage followed by a multi-phase buck converter stage for achieving high voltage gain, high current capability and good regulation [45-52]. Fig.1 shows the system architecture of this two-stage converter topology. The first stage is an unregulated switched-capacitor (SC) based converter. The second stage is a regulated high-frequency multi-phase DC-DC buck converter. As discussed in [46-48], an idealized model for a two-port switched-capacitor based DC-DC converter is made up of an ideal transformer with a turns ratio equal to the no-load conversion ratio, and an output resistance. The high voltage gain can be mainly achieved by the first stage converter while the accurate regulation and fast response can be realized by the second stage. Despite its advantages, this architecture suffers two major drawbacks: (i) there are many active and passive components in the two-stage converter, thus leading to a higher bill of materials (BOM) cost. (ii) with two switching stages (and higher switching losses due to more active switching devices used), the two-stage converter can significantly degrade

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efficiency.

Recently, hybrid single-stage converters have been proposed in [53] and [54] to achieve a high-voltage-gain step-down voltage conversion with reduced component count compared with two-stage converters. In the topology proposed in [53], a high conversion ratio with continuous input current is achieved and a novel resonant topology of step-down converter is proposed in [54]. However, a high voltage gain will lead to high power losses on the leakage inductors in these converters with single-stage structure.

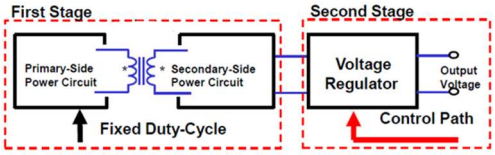

Fig. 1. Traditional two-stage high voltage gain DC/DC converter

In this paper, a high efficiency hybrid transformer-less DC/DC converter for high voltage gain and high current applications is proposed. The buck converter stage and SC converter stage are integrated into one stage with much fewer active switches and simpler gate driving circuits. The proposed hybrid DC/DC converter can achieve lossless regulation while maintaining both high efficiency and low cost. It features high step-down voltage conversion ratio with a moderate duty cycle; low voltage stress on all of the switches; easy implementation of control and driving circuits; scalability for high current and high-power applications; low cost due to reduced components via combination of a two-stage converter into single-stage converter. Interleaving control is adopted in the proposed converter to reduce the current ripple. Simulation and experimental results are shown to verify the functionality and demonstrate the superior performance of the proposed converter.

II. SYSTEM CONFIGURATION AND OPERATION PRINCIPLE OF THE PROPOSED DC-DC CONVERTER

In this section, descriptions of the system architecture and the modular structure of the proposed DC-DC switched-capacitor-buck converter are firstly given. The operating principle of the proposed converter is then discussed.

A. System Level Topology and Modular Structure

The topology of the proposed hybrid modular switched-capacitor-boost converter with high voltage gain is shown in Fig. 2. The analysis of the converter is based on the following assumptions.

1) All of the switching devices used in the proposed converter are ideal.
2) All input capacitors, DC flying capacitors and output capacitors have sufficiently large capacitance that will keep their holding voltages to be relatively constant throughout the operation, i.e., the voltage variation across the capacitors is neglected. Thus, these capacitors can be simply regarded as ideal voltage sources.
3) Compared with the conduction time of each active switch, the dead-time between the turning on of one switch and the turning off of a complementary switch, is very small and thus can be neglected. Therefore, to simply the analysis of circuit operation, no dead-time is considered.
4) When the proposed converter is working under steady state, the switching frequencies of all the switches in each module are the same.

The proposed converter comprises configurable N modules of switched-capacitor-boost circuits. Except for the first module which has no flying capacitor C_{B0}, all modules have two complementary MOSFETs, i.e., one flying MOSFET Φ_i (i=0, 1, 2, 3, …, N-1) and one bottom MOSFET $\bar{\Phi}_i$(i=0, 1, 2, 3, …, N-1), one power inductor L_i (i=0, 1, 2, 3, …, N-1), one input capacitor C_i (i=0, 1, 2, 3, …, N-1), and one flying capacitor $C_{B(i)}$ (i=1, 2, 3, …, N-1). Fig. 3 shows each module of switched-capacitor-boost circuit configuration in the proposed converter.

Here, v_{IN} and v_{OUT} are the input voltage and the output voltage of the proposed converter; $v_{B(i)}$ (i=1, 2, 3, …, N-1) are the voltages across the DC flying capacitors $C_{B(i)}$ (i=1, 2, 3,ss …, N-1) respectively and i_{Li} (i=0, 1, 2, 3, …, N-1) are the inductor currents corresponding to L_i(i=0, 1, 2, 3, …, N-1) respectively. The duty ratios of the flying MOSFETs Φ_i (i=0, 1, 2, 3, …, N-1) are denoted as d_i (i=0, 1, 2, 3, …, N-1), while the complementary duty ratios of the bottom MOSFETs $\bar{\Phi}_i$ (i=0, 1, 2, 3, …, N-1) are denoted as $\bar{d}_i$ (i=0, 1, 2, 3, …, N-1). Apparently, $d_i + \bar{d}_i = 1$.

To ensure voltage-second balance of all the inductors L_i (i=0, 1, 2, 3, …, N-1), the following equations to describe the steady-state operation can be derived.

$$\begin{cases} V_{IN} = \left[V_{B(i+1)} - V_{B(i)}\right] D_i \\ V_{B(N)} = V_{OUT} \\ V_{B0} = 0 \end{cases} \quad (i = 0,1,2,\ldots,N-1). \tag{1}$$

Based on (1), the voltage gain M_{Boost} of the proposed converter during steady-state operation can be derived as

$$M_{Boost} = \frac{V_{OUT}}{V_{IN}} = \sum_{i=1}^{N}\left(\frac{1}{D_i}\right) \quad (i = 1,2,3,\ldots,N). \tag{2}$$

To ensure charge balance of all flying capacitors $C_{B(i)}$ (i=1, 2, 3, …, N-1), the following steady state equation can be derived as

$$I_{L0}D_0 = I_{L1}D_1 = I_{L2}D_2 = \ldots = I_{L(N-1)}D_{N-1} \tag{3}$$

From (3), one can see that if the duty ratios of all flying MOSFETs are the same, then the steady-state current of each inductor will also be the same.

In general applications, the inductor currents are evenly distributed to achieve the merits of (i) modular design of the modules, which reduces the complexity of power converter system design; (ii) even thermal distribution. It is desirable to have even thermal distribution within the converter without having any hot spots. This means that the power stresses will be evenly distributed among the devices. It allows the converter to

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achieve maximum power delivery under a given thermal condition.

Therefore, the steady-state duty ratios D_i (i=0, 1, 2, 3, …, N-1) of all flying MOSFETs are set the same such that

$$D_0 = D_1 = D_2 = ...=D_{N-1}=D_{\text{Boost}} = D \tag{4}$$

where D_{Boost} or D is the unified duty ratio of the flying MOSFETs for achieving even current sharing condition.

Substitute (4) into (2),

$$M_{\text{Boost}} = \frac{V_{\text{OUT}}}{V_{\text{IN}}} = \frac{N}{D_{\text{Boost}}} \tag{5}$$

The voltage gain described in (5) is similar to that of a simple duty-cycle controlled N-phase boost converter that is embedded with a 1:N ratio switched-capacitor converter.

B. Operation Principle

To get maximum efficiency in conventional boost converters, the duty cycle should be close to 0.5 [4]. According to the design guideline in [55], the maximum duty cycle and the minimum duty cycle are both limited to achieve the optimization of the converter based on efficiency, cost, and volume. Therefore, the number of N could be calculated based on (5). In this study, the converter with four modules (N=4) is selected to illustrate the general operating principle. The optimization of the inductors, capacitors and power switches will be given in next section.

The converter with four modules (N=4) operating in steady-state operation is shown in Fig. 4(a), where the flying MOSFETs Φ_0 and Φ_2 are driven by signal PWM1, while Φ_3 and Φ_4 are driven by PWM2 that is out of phase with PWM1. Fig. 4(b) shows the corresponding timing diagram of the converter. Fig. 5 shows the equivalent circuits of the three operating states of the proposed converter.

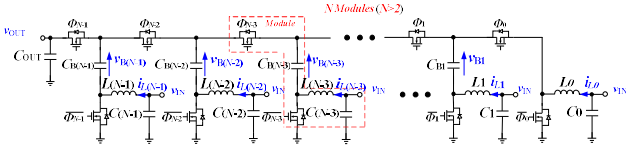

Fig. 2. System level configuration of the proposed converter.

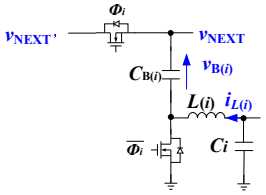

Fig. 3. Circuit configuration of each switch-capacitor-circuit module of the proposed converter.

In state I, all switches driven by PWM 1 are "ON" and all switches driven by PWM 2 are "OFF". Thus all switches driven by complementary of PWM 1 are "OFF" and all switches driven by complementary of PWM 2 are "ON". V_{IN} charges the flying capacitor C_{B2} through inductor L_1, and output capacitor C_{OUT} through inductor L_3, respectively, as illustrated in Fig. 5(a). Concurrently, the flying capacitors C_{B1} and C_{B3} are discharging to C_{B2} and C_{OUT}, respectively. In the meantime, inductors L_0 and L_2 are both charged by V_{IN} and energy is stored in these two inductors. The load is supplied by the voltage across C_{OUT}.

In state II, all switches driven by PWM 1 are "OFF" and all switches driven by PWM 2 are "ON". Thus all switches driven by complementary of PWM 1 are "ON" and all switches driven by complementary of PWM 2 are "OFF". V_{IN} charges the flying capacitor C_{B1} through inductor L_0, and the flying capacitor C_{B3} through inductor L_2, respectively, as illustrated in Fig. 5(b). Concurrently, the flying capacitors C_{B2} and C_{OUT} are discharging to C_{B3} and the load, respectively. In the meantime, inductors L_1 and L_3 are charged by V_{IN} and energy is stored in these two inductors.

In state III, all switches driven by PWM 1 are "OFF" and all switches driven by PWM 2 are "OFF". Thus all switches driven by complementary of PWM 1 are "ON" and all switches driven by complementary of PWM 2 are "ON". Since all of the flying MOSFETs are turned off, the flying capacitors are neither charging nor discharging. The inductor L_0 - L_3 are all charged by V_{IN} and energy is stored in these inductors. Concurrently, the load is supplied by the voltage across C_{OUT}, as illustrated in Fig. 5(c).

According to (4), assuming that the steady-state duty ratios D_i (i=0, 1, 2, 3) of all flying MOSFETs are set the same and equal to D to achieve even current sharing condition of all the inductors L_0-L_3, the following equations for the steady-state operation can be derived.

$$\begin{cases} (V_{\text{OUT}} - V_{\text{B3}})D = V_{\text{IN}} \\ (V_{\text{B3}} - V_{\text{B2}})D = V_{\text{IN}} \\ (V_{\text{B2}} - V_{\text{B1}})D = V_{\text{IN}} \\ V_{\text{B1}}D = V_{\text{IN}} \end{cases} . \tag{6}$$

Then, (6) is further simplified as

$$\begin{cases} V_{\text{B1}} = \dfrac{V_{\text{IN}}}{D} \\ V_{\text{B2}} = 2\cdot\dfrac{V_{\text{IN}}}{D} \\ V_{\text{B3}} = 3\cdot\dfrac{V_{\text{IN}}}{D} \\ V_{\text{OUT}} = 4\cdot\dfrac{V_{\text{IN}}}{D} \end{cases} . \tag{7}$$

According to (7), different DC flying capacitors $C_{\text{B}(i)}$ (i=1, 2, 3) have different DC voltage offset $V_{\text{B}(i)}$ (i=1, 2, 3) in this converter, which is similar to that of traditional switched-capacitor based converters.

Based on (7), the voltage gain M of the proposed converter with four modules (N=4) during steady-state operation can be derived as

$$M = \frac{V_{\text{OUT}}}{V_{\text{IN}}} = \frac{4}{D} \tag{8}$$

which matches (2) for the case N=4.

From the operation principle illustrated above, every flying capacitor is always being softly charged or softly discharged during the operation [56], thereby minimizing the effect of the power loss of the converter due to voltage ripple fluctuation of

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the flying capacitors. This is due to the hybrid structure of the proposed converter that couples the boost inductor into the switched-capacitor stage. This critical feature will eliminate the inrush current in traditional switched-capacitor based converters. Therefore, the inherent charge sharing losses during the charging and discharging processes of capacitors, are avoided. For this reason, the soft-charging of the proposed hybrid converter is ensured regardless of the tolerance of flying capacitors.

With four modules (N=4), the proposed converter is equivalent to a 4-phase interleaved boost converter embedded with a 1:4 switched capacitor converter. Therefore, the small-signal plant model of the proposed converter can be simply modelled as a conventional boost converter cascaded by a 1:4 gain. The controller design is thus quite similar to that of the (4-phase interleave) boost converter and is well documented in literature [57]. This converter can be obtained by inverting the power flow direction of a multiphase version of the series capacitor buck converter as reported in [59], where voltage regulator (VR) and point of load applications are the main research objectives.

C. Interleaving Operation

To cancel out the input current ripple, interleaving control is adopted in the proposed converter. With a proper management of gate driving signals, the proposed four-module converter with 360/4 degree interleaving between each module can be realized. The timing diagram of the flying MOSFET Φ_i (i=0, 1, 2, 3) gate signals for perfect interleaving operation is shown in Fig. 6. This circuit can be considered as a combination of 4-phase interleaved traditional boost converter and a four-module switched capacitor converter. This will achieve 4-phase input current ripple cancellation and significantly reduces the input current ripple. Therefore, the current stress on the input capacitor can be reduced, and the huge input capacitor bank typically required to buffer the large input current ripple can be eliminated.

D. Duty Ratio Limitation

According to the operation principle, for the proposed converter with configurable N modules, it is obvious that the neighboring on-time of the flying MOSFETs cannot be overlapped, i.e.,

$$D_{i-1} + D_i \le 1 \quad (i = 0,1,2,...,N-1) \tag{9}$$

Substitution of (4) into (9) gives

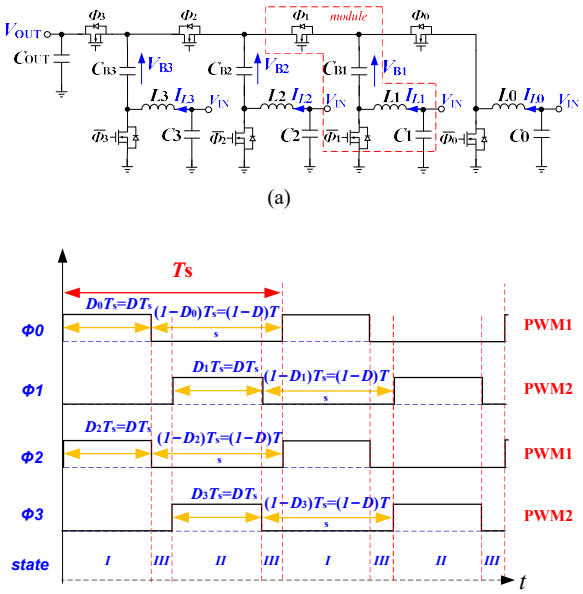
$$D_i \le 0.5 \quad (i = 0,1,2,...,N-1) \tag{10}$$

which means the duty ratios of the flying MOSFETs of the proposed converter must be less than 0.5. Substitute (10) into (2),

$$V_{OUT} \ge 2NV_{IN} \tag{11}$$

Apparently, the minimum output voltage of the proposed converter is $2NV_{IN}$ for the boundary case of D_i (i=0, 1, 2, 3, … , N-1).

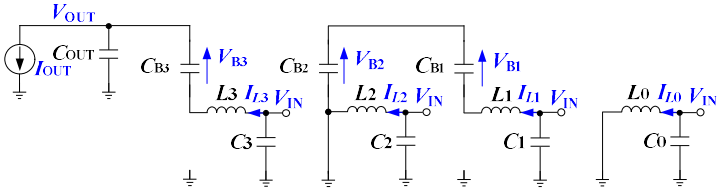
Normally, the voltage conversion ratio of conventional boost DC/DC converter is limited to five times because of the large power losses at the extreme duty cycle condition with high voltage gain [4]. Therefore, according to (5), the maximum output voltage of the proposed converter is $5NV_{IN}$ in practical sense. Hence, the output voltage range of the proposed converter is from $2NV_{IN}$ to $5NV_{IN}$.



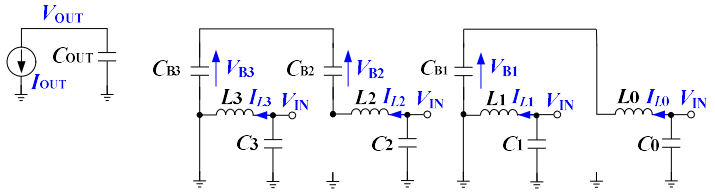
(a)

(b)

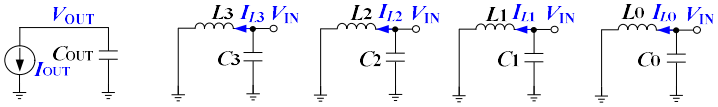
Fig. 4. (a) The proposed converter with four modules (N=4) and (b) its timing diagram



(a) State I



(b) State II



(c) State III

Fig. 5. Equivalent circuits of the three different operating states for each phase.

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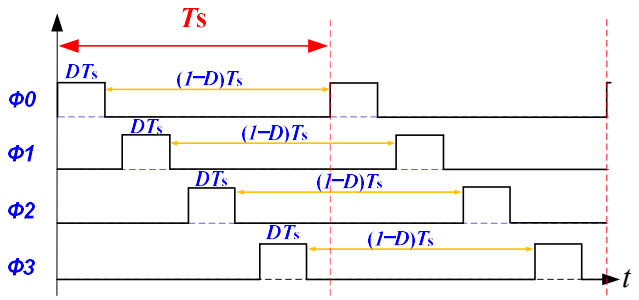

Fig. 6. Timing diagram of the flying MOSFET Φ_i (i=0, 1, 2, 3) gate signals with perfect interleaving operation on proposed converter with four modules(N=4).

III. CIRCUIT DESIGN AND OPTIMIZATION

A. Selection of the Power Components

Five parameters are necessary to initiate a converter design: Input voltage (V_{IN}), output voltage (V_o), maximum output current (I_{O_MAX}), the number of modules in the converter (N), and the switching frequency (f_s). With these given parameters, the components' design and optimization can be completed, as illustrated in the following.

i. Inductor:

Assuming that the switches of the converter are all ideal, the inductance of each module can be calculated from

$$L=\frac{V_{IN}\cdot(1-D)}{\Delta I_L\cdot f_s} \tag{12}$$

where inductor current ripple $\Delta I_L=\alpha\cdot I_{O\_MAX}$, and α is typically chosen as 0.2~0.3.

ii. Flying Capacitor:

Due to the special structure of the proposed converter, the voltage ripple across all of the flying capacitors are the same if the flying capacitance of each module is the same.

Assuming that the current ripple of each inductor L_i (i=0, 1, 2, 3, …, N-1) is neglected, the capacitance of flying capacitor in each module can be calculated from

$$C=\frac{P_{OUT\_MAX}\cdot D}{\Delta V_C\cdot V_{IN}\cdot N\cdot f_s} \tag{13}$$

where ΔV_C is the voltage ripple across each flying capacitor $C_{B(i)}$ (i=1, 2, 3, …, N-1). The capacitance of the flying capacitor is determined by the desired voltage ripple, number of modules, duty cycle of flying active switches, input current at full load and switching frequency. To obtain a higher efficiency, the voltage ripple should be as low as possible. A proper value of the flying capacitor will improve the efficiency.

According to (13), the flying capacitor is calculated to be around 47 μF given a peak-to-peak capacitor voltage ripple of 1.33 V. This voltage ripple is negligible to their DC value, so that the flying capacitors can be effectively regarded as a constant voltage source/sink. In most DC-DC converter topologies, the electrical characteristics like power losses, input and output impedance, etc, are often associated with the capacitor values. The low equivalent-series-resistance (ESR) Class-II multi-layer ceramic capacitors (MLCCs) can be used to achieve low voltage ripple across the DC flying capacitors. In addition, class-II MLCCs can usually offer high capacitance per volume to achieve higher power density. In this hardware prototype, class-II (e.g., X7R, X6S, etc.) high current rating MLCC capacitors are used as flying capacitors. If the current rating of one capacitor chosen cannot meet the current requirement, then more capacitors can be used in parallel. In this prototype, ten 4.7 μF MLCCs are used in parallel to obtain the required total 47 μF capacitance for each module. The current rating of each MLCC is 3A. As illustrated previously, different DC flying capacitors $C_{B(i)}$ (i=1, 2, 3, …, N-1) have different DC voltage offset in this converter. If the capacitance for each flying capacitor is kept the same, those capacitors with higher DC voltage offset may be of larger size.

iii. Switch:

Basically, the maximum voltage of all switches can be determined using a scaling function of N. The current ratings of all switches can be determined by its corresponding inductor peak current, as shown in Table I.

In a Dickson based step-up switched-capacitor converter (SCC) topology [16], all switching devices are only seeing either V_{OUT}/N or $2(V_{OUT}/N)$ during normal operation, which means they require only low voltage rating MOSFETs with better figure of merits (FOMs). Similarly, one of the key enabler for the proposed hybrid converter is the opportunity to use low voltage rating MOSFETs with better FOMs. At any switching state, all of the OFF switches are always clamped at either V_{OUT}/N or $2(V_{OUT}/N)$ (for step-up/boost case) by the DC flying capacitors and input/output capacitors. This ensures the reliable use of low voltage rating devices with minimal voltage stresses and superior FOMs. Existing solutions are all using high-performance silicon-based MOSFETs instead of GaN MOSFETs. Therefore, for a fair comparison, silicon-based MOSFETs are chosen for the hardware prototype.

In the case when there are N modules embedded in the converter and thus the conversion ratio is equal to N/D, the total device number is $2N$, including N flying MOSFETs Φ_i (i=0, 1, 2, 3, …, N-1) and N bottom MOSFETs $\overline{\Phi}_i$ (i=0, 1, 2, 3, …, N-1).

Table I. VOLTAGE STRESS AND CURRENT STRESS OF SWITCHES

MOSFET	Voltage Stress	Current Stress
Φ_{N-1}	(V_{OUT}/N)	Peak of $I_{L(N-1)}$
Φ_i (i=0, 1, 2, …, N-2)	$2(V_{OUT}/N)$	Peak of I_{Li} (i=0, 1, 2, …, N-2)
$\overline{\Phi_i}$ (i=0, 1, 2, …, N-1)	(V_{OUT}/N)	Peak of I_{Li} (i=0, 1, 2, …, N-1)

Due to the better utilization of switches in the topology as shown in Table I and the full leverage of the superior FOMs of low voltage rating MOSFETs, this topology is particularly compelling for high-voltage gain, high current applications. Based on the calculated values of the components illustrated above, real components of hardware prototype are selected for the optimization of the proposed converter.

B. Design of the Gate Driving Architecture

In the case when there are N modules embedded in the

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converter, N high-side and N low-side MOSFETs are needed. The design of the gate drivers for the low-side MOSFETs are straightforward as all MOSFETs are sourced to the common ground. Gate driving for the four high-side MOSFETs are challenging, as the conventional transformer-based gate driving techniques are bulky, and the conventional bootstrap circuit will lead to uneven gate driving voltage (as the high-side MOSFETs are stacked up in a series configuration) and/or may require a dedicated startup sequence of the MOSFETs before the bootstrap capacitors can be charged up.

The proposed gate driving circuit for the high-side MOSFETs are shown in Fig. 7. It is a simple and scalable charge pump circuit and designed to generate bias power for each floating MOSFET. The proposed charge pump circuit utilize two small capacitors (C_1 and C_2), three diodes ($D_1 - D_3$), and two transistors Q_1 and Q_2. The capacitors are used to transfer energy to the floating high-side switch from a single power supply V_{drive} referred to the ground. Schottky diodes are used for $D_1 - D_3$ because of their low voltage drops and less conduction losses. Q_1 and the high side MOSFET are driven by two complementary signals, $\overline{\text{PWMx}}$ and PWMx, respectively. Q_2 is turned on/off automatically as Q_1 is turned off/on.

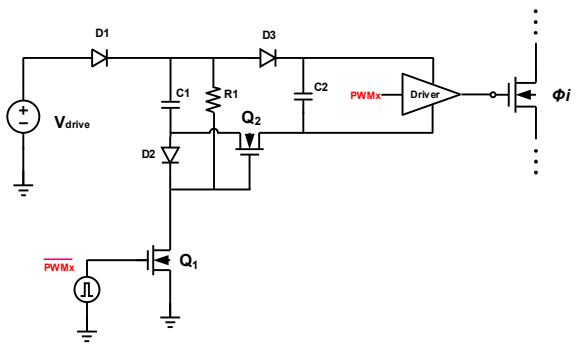

Fig. 7. Proposed gate driving method for high side MOSFETs (per module).

IV. SIMULATION AND EXPERIMENTAL RESULTS

Simulation has been conducted to verify the performance of the proposed hybrid DC/DC converter with four modules (N=4) in the interleaved operation. The parameters used in the simulation is shown in Table II. The input voltage of the prototype is 2.5 V. The output voltage is 48 V, which is a typical DC bus voltage for low voltage DC micro-grids. The full output power is 300 W. Fig. 8(a) shows the current waveforms of L_1-L_4 at full load (300 W output power). Fig. 8(b) shows voltage across FET Φ_3 and $\overline{\Phi_3}$. Fig. 8(c) shows the output voltage and voltage waveforms of capacitors C_{B1}- C_{B3}. With an output voltage of 48 V, the average voltage on C_{B1}- C_{B3} are 12 V, 24 V and 36 V respectively, as expected in (7). The input current at full load are also simulated, as shown in Fig. 8(d). According to Table I, the maximum voltage stress on FET Φ_3 and $\overline{\Phi_3}$ is 12 V, which matches the simulated result. Fig. 8(e) shows the simulated input current waveform in the non-interleaved operation under the same operating condition. From the simulated results shown in Fig. 8 (d) and (e), one can see that under the same operating condition, input current ripple is about 6 A in the non-interleaved operation while the input current ripple can be reduced to as low as 0.8 A in the interleaved operation. Therefore, due to the interleaved operation, the input current ripple has been reduced a lot.

To validate the operating principle and design of the proposed hybrid DC/DC converter, one prototype with N=4, i.e. four modules enabled, as shown in Fig. 9, has been built. The prototype consists of two PCB boards, namely, a DSP control board, a power stage board. And the power stage board consist of six modules. With four modules enabled and other two modules disabled, the board can work in a four-module operation. A detailed list of components used in the hardware prototype is shown in Table III. The closed-loop digital controller is implemented using DSP TMS320F28335. The MOSFETs used are BSC009NE2LS5. The rated voltage of the MOSFET is 30 V, and the turn-on resistance is below 1mΩ. The MOSFET drivers and control logic circuitries can be further fabricated and integrated into a semiconductor chip to offer a more compact solution. The test condition is same as that in the simulation, as shown in Table II.

Fig. 10 shows the measured voltage and current waveforms of the proposed converter during steady-state non-interleaved operation, as illustrated in previous section II (B). Fig. 10(a) shows the measured PWM signal and the complementary PWM signal of flying MOSFETs Φ_0. Other three PWM signals of flying MOSFETs Φ_i (i= 1, 2, 3) are the same as PWM signal of flying MOSFETs Φ_0. Fig. 10(b) shows the measured waveforms of voltages on capacitors C_{B1}- C_{B3} and output voltage V_{OUT}. As shown, the average voltage on C_{B1}- C_{B3} are 12 V, 24 V and 36 V respectively, which match the analytical results. Fig. 10(c) and (d) show the current waveforms of L_0-L_3. Fig. 10(e) shows the waveforms of the drain-to-source voltage across device Φ_1 and $\overline{\Phi_1}$. The above results show that the operation of proposed converter matches the analytical results.

Fig. 11 shows the measured voltage and current waveforms of the proposed converter during steady-state interleaved operation, as illustrated in previous section II (C). Fig. 11(a) shows the measured PWM signals of four flying MOSFETs Φ_i (i=0, 1, 2, 3). Fig. 11(b) shows the measured waveforms of voltages on capacitors C_{B1}- C_{B3} and output voltage V_{OUT}. As shown, the average voltage on C_{B1}- C_{B3} are 12 V, 24 V and 36 V respectively, which match the analytical results. Fig. 11(c) shows the current waveforms of L_0-L_3. Fig. 11(d) shows the waveforms of the drain-to-source voltage across device Φ_1 and $\overline{\Phi_1}$. The above results show that the proposed converter can achieve 4-phase interleaved operation to improve cancellation of input current ripple. This matches the simulated results.

Fig. 12 shows the measured voltage and current waveforms of the proposed converter during transient step-load operation with a closed-loop controller. A closed-loop voltage mode controller is utilized. The waveforms of load current, output voltage and PWM signal of MOSFET Φ1 are measured. The fluctuation of output voltage is about 0.6 V when the load step change from 150 W to 300 W. There is no oscillation at the

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output voltage. The above results show that the proposed converter can achieve smooth output transient response.

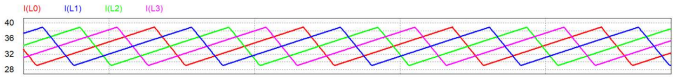
Both results of measured efficiency and calculated efficiency of the proposed converter in the interleaved operation are plotted as shown in Fig. 13. To get the most accurate measured results, Fluke multimeters in high-resolution mode are used to measure the input voltage, output voltage and input current. Chroma programmable loads are used to measure the output current. As shown in Fig. 13, the measured peak efficiency of the converter is 96.1% while the calculated peak efficiency is 96.5%. The measured full load efficiency of the converter is 94.1% while the calculated full load efficiency is 95.2%. It can be seen that there is a slight discrepancy between the calculated efficiencies and the measured efficiencies. This is attributed to non-accurate conduction resistance given in the datasheets of components and unknown PCB resistance. Fig. 14 shows the calculated power loss breakdown of MOSFETs at output voltage of 48 V and output power of 300 W in the interleaved operation.

Table II. PARAMETERS USED IN THE SIMULATION

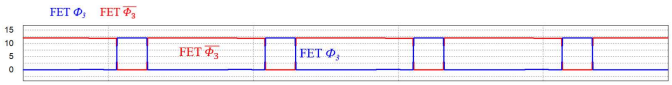
Description	Items	Values
Input Voltage	V_{IN}	2.5 V
Output Voltage	V_{OUT}	48 V
Output Power	P_{OUT}	300 W
Flying Capacitor	$C_{B1\text{-}B3}$	47 μF
Inductor	$L_{0\text{-}3}$	2 μH
Resistor Load	R_{OUT}	7.68 Ohm
Switching Frequency	F_{SW}	100 kHz

Table III. COMPONENTS USED IN THE PROTOTYPE

Description	Part#
Digital Controller	TMS320F28335
Flying Capacitor *CB3*	C3216X7R1H475K160AC
Flying Capacitor *CB2*	C3216X7R1H475K160AC
Flying Capacitor *CB1*	C3216X7R1H475K160AC
Inductor	744323020 (0.2 µH)
Switching Device	BSC009NE2LS5
Level Shifter	ADUM5240
Gate Driver	LTC4440

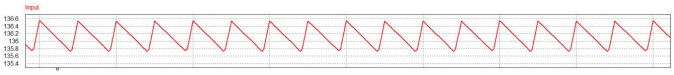


(a) Inductor L_0-L_3 Current (A)

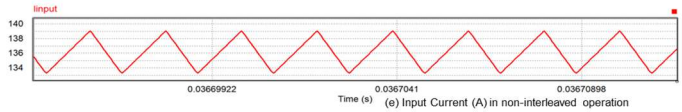


(b) Device Φ_3 and $\overline{\Phi_3}$ drain-to-source Voltage (V)

(c) Converter Capacitor C_{B1}- C_{B3} Voltage and Output Voltage (V)



(d) Input Current (A)



(e) Input Current (A) in non-interleaved operation

Fig. 8. (a)-(d) Simulated results of the proposed converter in the interleaved operation with 2.5 V input and 48 V output operating at 300 W; (e) Simulated input current waveform in the non-interleaved operation under the same operating condition.

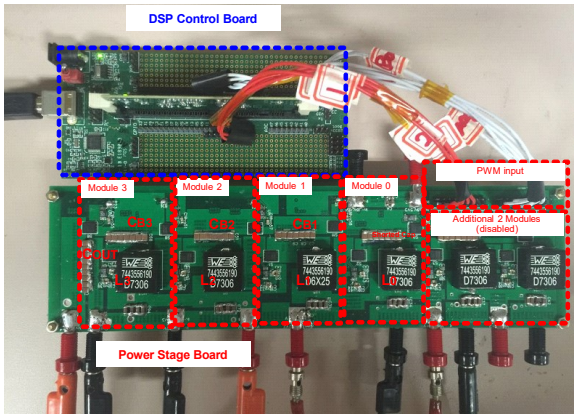
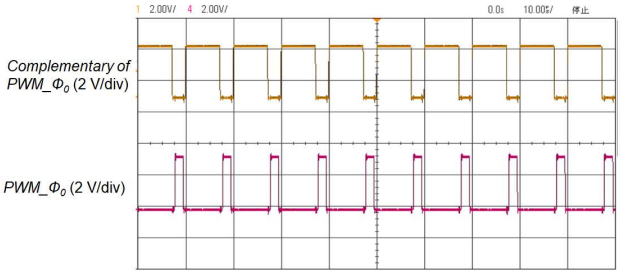


Fig. 9. Hardware prototype of the proposed converter with four modules enabled.



(a)

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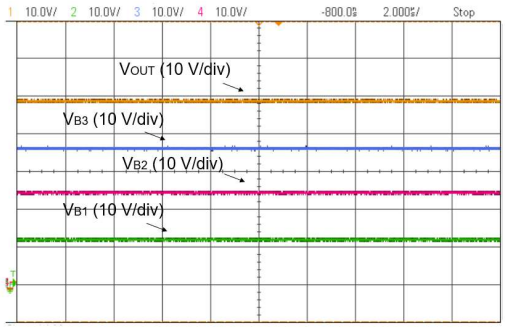

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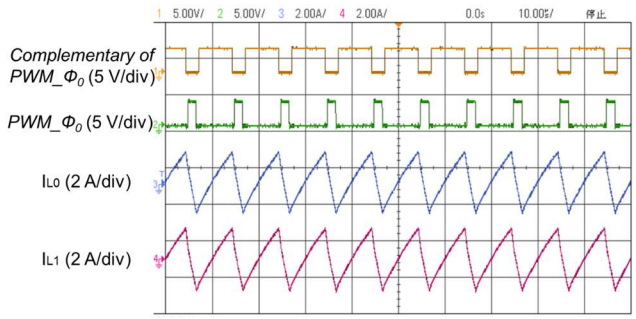

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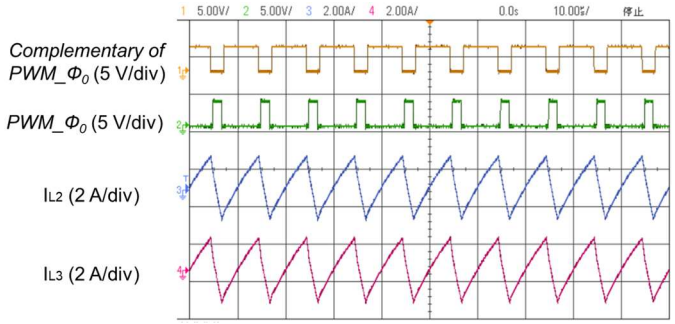

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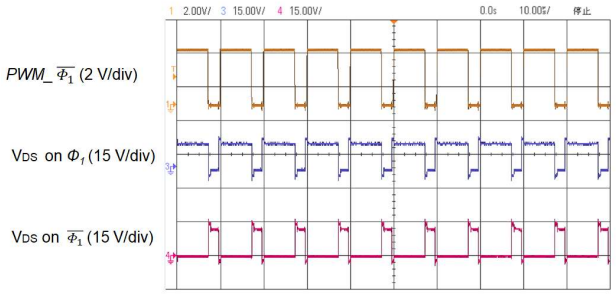
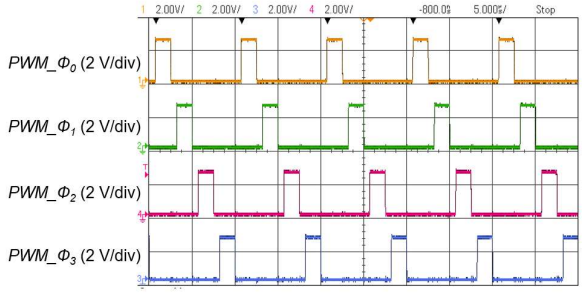


(e)

Fig. 10. Measured operating waveforms in the non-interleaved operation (a) PWM signal and complementary PWM signal of flying MOSFETs Φ_i (i=0) (b) voltages on capacitors C_{B1}- C_{B3} and output voltage V_{OUT} (c) current of inductors L_0-L_1 (d) current of inductors L_2-L_3 (e) drain-to-source voltage across device Φ_1 and $\overline{\Phi_1}$.



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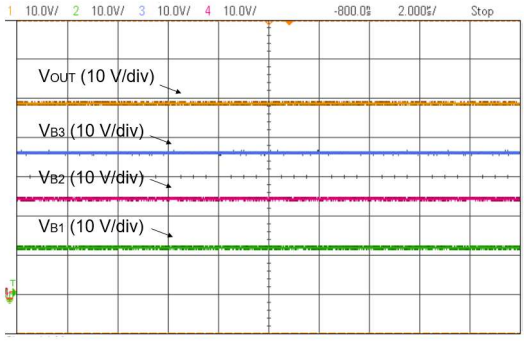

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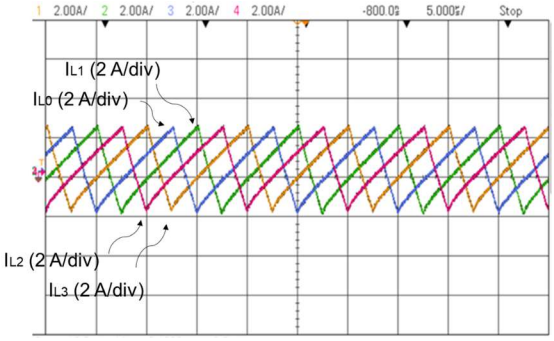

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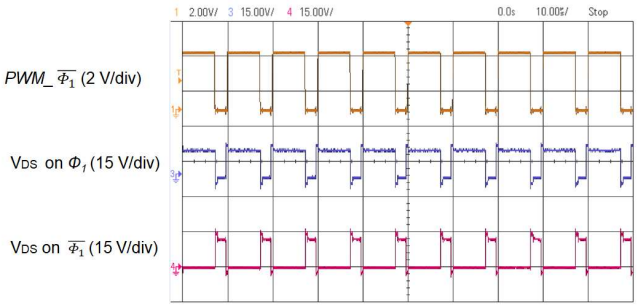

(d)

Fig. 11. Measured operating waveforms in the interleaved operation (a) PWM signals of four flying MOSFETs Φ_i (i=0, 1, 2, 3) (b) voltages on capacitors C_{B1}- C_{B3} and output voltage V_{OUT} and (c) current of four inductors L_0-L_3 (d) drain-to-source voltage across device Φ_1 and $\overline{\Phi_1}$.

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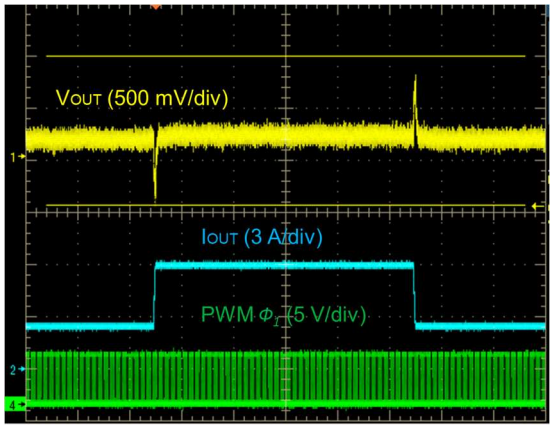

Fig. 12. Measured step load operating waveforms.

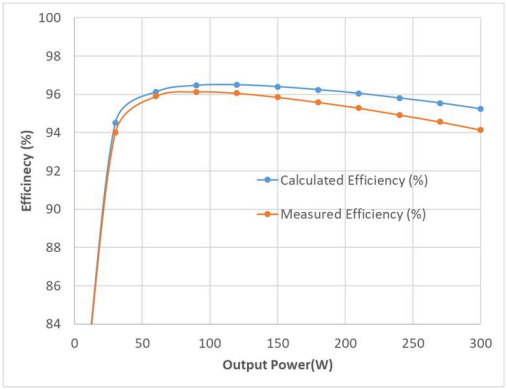

Fig. 13. Both results of the measured efficiency and calculated efficiency of the proposed converter in the interleaved operation.

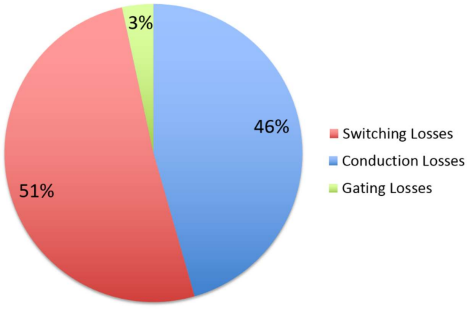

Fig. 14. Calculated power loss breakdown of MOSFETs at output voltage of 48 V and output power of 300 W.

V. A COMPARISON OF DIFFERENT HIGH-VOLTAGE-GAIN CONVERTERS

As discussed in the previous section, one common solution for high-voltage-gain step-up conversion is to adopt two-stage DC/DC conversion, which consists of a high voltage gain SC converter stage followed by a conventional multi-phase boost converter stage for concurrently achieving high voltage gain, high current capability and good regulation. Fig. 15(a) shows a typical two-stage solution with high-voltage-gain step-up conversion in high current and high-power applications. The first stage is a 1:4 switched-capacitor converter and the second stage is a 4-phase boost converter. This two-stage converter is conventional for high voltage gain and high-power applications. The 4-phase operation in boost converter can realize accurate regulation with fast response, and easily handle high power and high current stresses as compared with single-phase boost operation [58]. The proposed converter with the same voltage gain and the same power rating is given to have a fair comparison with the two-stage solution, as shown in Fig. 15(b). With the same voltage gain and the same power rating, there are altogether 18 active switches in the two-stage solution while there are 8 active switches in the proposed hybrid converter. As the proposed converter is derived from the hybrid integration of the switched-capacitor converter and the boost converter, and many active switches of the two separate stages are merged together, all the active switches of the switched-capacitor converter stage are saved, leading to a lower bill of materials (BOM) cost. In addition, with only one group of active switches (due to one switching stage) and lower switching losses (due to fewer switching devices used), the proposed hybrid single-stage converter can achieve a significantly improved efficiency. Besides, the performance of the proposed converter is compared with that of other single-stage converters [51-54], as shown in Table. IV. It is shown that the proposed converter can achieve a higher efficiency even at a higher voltage gain.

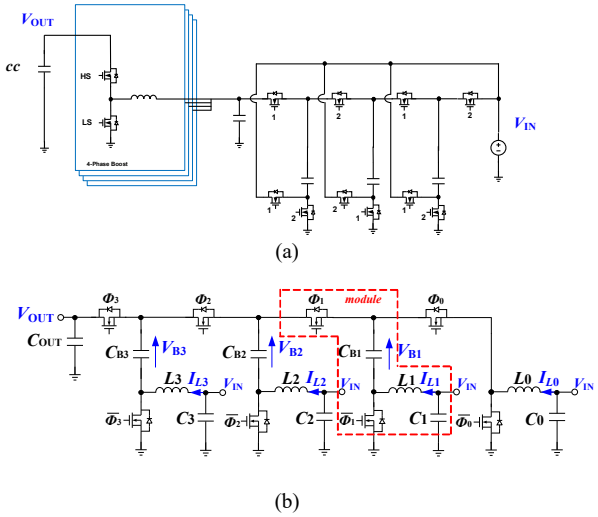

Fig. 15. (a) Typical two-stage solution with high-voltage-gain step-up conversion in high current and high-power applications. (b) Proposed converter.

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Table IV. COMPARISONS FOR DIFFERENT HIGH-VOLTAGE-GAIN CONVERTERS

The converter in	Voltage Gain (times)	Output Power (W)	Switching Frequency (kHz)	Peak Efficiency (%)	Switch	Transformer?	Low voltage stresses?	Scalability
[51]	15	2000 W	100	90%	10	Yes	No	Medium
[52]	15	2000 W	100	92%	8	Yes		Medium
Proposed	15	2000 W	100	96.9%*	8	No	Yes	Very good
[53]	16.6	100 W	100	90%	4	Yes	No	Poor
Proposed	16.6	100 W	100	96.7%*	8	No	Yes	Very good
[54]	16.6	300 W	100	94.5%	1	Yes	No	Poor
Proposed	19	300 W	100	96.1%	8	No	Yes	Very good
Cascaded boost	19	300 W	100	92.0 %	10	No	No	Medium

*Estimated based on loss model

VI. CONCLUSIONS

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This paper presents a new class of high frequency DC-DC converter for high efficiency transformer-less DC-DC application where large voltage step-down ratios are required.

All of the features can be concluded as follows.

1) Regulated high step-down voltage conversion ratio with a moderate duty cycle.

2) High efficiency due to fewer MOSFETs in the merged single stage and utilization of low-voltage high-performance switching devices, thus suitable for high frequency operation.

3) Non-pulsating current and reduced current ripple due to interleaved operation.

4) Relatively low overall cost due to hybrid structure with fewer MOSFETs and combination of two-stage converter into single-stage converter.

5) Inherent modular structure and scalability for high current high power application.

6) Reduction of the current and voltage spike problems and EMI issues due to full soft charging operation of the flying capacitors

Steady-state operations of the proposed converter were analyzed in the paper. A prototype of a 2.5 V-to-48 V 300 W converter was designed and built to demonstrate the advantages of the proposed topology, and it achieved a peak efficiency of 96.1%. Both simulation and experimental results validated the theoretical analysis.

The proposed converter can be widely used as an interface for renewable energy systems in DC micro-grids. The proposed converter also shows great potential in high voltage gain, high current and high power applications. Therefore, the proposed hybrid converter can be applied to a broad range of power conversion utilizations.

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